AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A serial communication device, comprising:

a serial interface to receive data; and

a direct memory access controller to transfer said data received by said serial interface from said serial interface to a first memory external to the direct memory access controller,

wherein said direct memory access controller is started up before said serial interface receives said data,

said direct memory access controller sets a number larger than the number of data received at a time by the serial interface as a number of transfers to said first memory before said serial interface receives said data, and

when the number of data transferred from said serial interface to said first memory reaches said number set as the number of transfers, said direct memory access controller outputs a direct memory access transfer end interrupt signal to a central processing unit.

Claim 2 (cancelled)

3. (previously presented) The serial communication device according to claim 1, wherein said serial interface outputs a receive timeout interrupt signal to said central processing unit when said data reception is stopped for a certain period after the start of said data reception.

4. (original) The serial communication device according to claim 3, wherein said direct memory access controller retransfers said transferred data from said first memory to a second memory as triggered by said direct memory access transfer end interrupt signal or said receive timeout interrupt signal.

5. (currently amended) The serial communication device according to claim 1,

wherein said first memory is comprised of two or more memory areas, and

said direct memory access controller has a continuous transfer function and transfers said data from said serial interface to said first memory while alternately switching the destinations of the data received by said serial interface among said two or more memory areas, as triggered

by said direct memory access transfer end interrupt signal or a receive timeout interrupt signal.